IN THE CLAIMS:

1. (Currently Amended) In a system in which an ATM slave processing unit is coupled to an ATM master processing unit by a communication bus, the interaction between the ATM master processing unit and the ATM slave processing unit having a UTOPIA format, an ATM slave interface unit providing an interface between the communication bus and a direct memory access unit coupled to the ~~an~~ ATM slave processing unit, the interface unit comprising:

an input unit, the input unit receiving data cells and exchanging control signals with the ATM master processing unit;

an input buffer unit receiving data signals and exchanging control signals with the input unit, the input buffer unit including:

a buffer storage unit coupled to the input unit, the buffer storage unit being a first-in/first-out memory unit configured to store two data cells received from the input unit to permit the data cells to be transferred on consecutive clock cycles to a destination location when the destination location is available, the buffer storage unit transferring data cells to the direct memory access unit in response to a first READY signal; and

a calculation unit;

a register, each data cell including a cell portion having the destination location encoded therein, the calculation unit responsive to the contents of the register and to the cell portion for generating the destination location for the data cell in the ATM slave processing unit;

an output buffer unit, the output buffer unit being a first-in first-out storage unit for storing data cells, the output buffer unit receiving data cells from the direct memory access unit in response to a second READY signal and exchanging control signals with the direct memory access unit; and

an output unit, the output unit receiving data cells from the output buffer unit and applying data cells to the communication bus, the output unit exchanging control signals with the ATM master processing unit.

Claims 2-3 (Canceled)

4. (Original) The interface unit as recited in claim 1 wherein the buffer storage unit transfers a data cell to the slave data processing unit every clock cycle.

5. (Previously Presented) The interface unit as recited in claim 1 wherein the destination locations are selected from at least one of the group consisting of a slave processing unit, shared memory locations for a plurality of slave processing units, and at least one slave processing unit and at least one shared memory location.

6. (Canceled)

7. (Original) The interface unit as recited in claim 1 wherein the ATM slave processing unit includes at least one digital signal central processing unit.

Claims 8-9 (Canceled)

10. (Currently Amended) A method for exchanging data cells from an ATM master processing unit with a plurality of locations in an ATM slave processing unit, over a communication bus, the ATM slave processing unit coupled to ~~including~~ a direct memory access unit, the method comprising:

storing data cells from the ATM master processing unit in a buffer storage unit coupled to the communication bus, wherein the buffer storage unit is a first-in/first-out storage unit configured to store two of the data cells to permit the data cells to be transferred on consecutive clock cycles to a destination location;

generating ~~comparing a field in the data cell with the contents of a register to determine~~ the destination location for each of the data cells in the buffer storage unit responsive to the contents of the register and to a cell portion included in each of the data cells that has the destination location encoded therein ~~of each data cell~~;

generating a signal identifying the destination location;

when storage space is available, transferring a data cell from the buffer storage unit to the direct memory access unit in response to a first READY signal;

storing data cells in a output buffer unit received from the direct memory access unit in response to a second READY signal, wherein the output buffer unit is a first-in first-out storage unit and is configured to exchange control signals with the direct memory access unit; and

receiving data cells at an output unit from the output buffer unit and applying data cells to the communication bus from the output unit, the output unit configured to exchange control signals with the ATM master processing unit.

11. (Previously Presented) The method as recited in claim 10 further comprising:

transferring a data cell from the buffer storage unit to the ATM slave processing unit on consecutive clock cycles.

12. (Previously Presented) The method as recited in claim 11 further comprising implementing the signals exchanged over the communication bus in a UTOPIA format.

13. (Previously Presented) The method as recited in claim 10 wherein the method includes applying the signal identifying the destination location to the direct memory access unit.

14. (Currently Amended) A data processing system comprising:

an ATM master processing unit;

a communication bus coupled to the ATM master processing unit;

an ATM slave processing unit, the ATM slave processing unit coupled to the ATM master processing unit via the communication bus and coupled to ~~including~~ a direct memory access unit; and

an ATM slave interface unit providing an interface between ~~coupled to~~ the communication bus and the direct memory access unit, the slave interface unit including:

an input unit, the input unit receiving data cells and exchanging UTOPIA format signals with the ATM master processing unit;

an input buffer ~~storage unit, the input buffer~~ unit receiving data ~~cell~~ signals and exchanging control signals with ~~from~~ the input unit, the input buffer unit including:

a buffer storage ~~memory~~ unit coupled to the input unit, the buffer storage ~~memory~~ unit being a first-in/first-out memory ~~storage~~ unit configured to store two data cells received from the input unit ~~of the data cell signals~~ to permit the data cells to be transferred on consecutive clock cycles to a destination location when the destination location is available, the buffer storage ~~memory~~ unit transferring ~~the~~ data cells to the direct memory access unit in response to a first READY signal; and

a calculation unit;

a register, each data cell including a cell portion having the destination location encoded therein, the calculation unit responsive to the contents of the register and to the cell portion for generating the destination location for the data cell in the ATM slave processing unit ~~the contents of the register identifying a destination location field in a data cell, the contents of the register providing the translation of the field in the data cell into a destination~~

~~location, wherein the calculation unit generates a destination location signal and applies the destination location signal to the direct memory access unit~~;

an output buffer unit, the output buffer unit being a first-in first-out storage unit for storing data cells, the output buffer unit receiving data cells from the direct memory access unit in response to a second READY signal and exchanging control signals with the direct memory access unit; and

an output unit, the output unit receiving data cells from the output buffer unit and applying data cells to the communication bus, the output unit exchanging UTOPIA format signals with the ATM master processing unit.

Claims 15-17 (Canceled)

18. (Previously Presented) The interface unit as recited in claim 1 wherein the interface unit operates at a first frequency and the direct memory access unit operates at a second frequency.

19. (Previously Presented) The interface unit as recited in claim 18 wherein the first frequency is a UTOPIA clock frequency.